AMENDMENTS TO THE CLAIMS

Claims 1 – 42 (Canceled)

Claim 43 (Original) A method of fabricating an integrated circuit, comprising:

providing a substrate, said substrate comprising a switch and a first insulator layer covering said switch;

forming a nonconductive buried diffusion barrier layer on said first insulator layer; and

forming a second insulator layer on said nonconductive buried diffusion barrier layer.

Claim 44 (Original) A method as in claim 43, further comprising:

forming a conductive plug with a bottom end and a top end, said bottom end in electrical contact with said switch;

planarizing said top end and said second insulator layer;

forming a conductive oxygen-diffusion barrier layer on said second insulator layer and on said top end of said conductive plug;

forming a bottom electrode layer on said conductive oxygen-diffusion barrier layer;

forming a dielectric thin film on said bottom electrode layer;

forming a top stack-electrode layer on said dielectric thin film; and

removing portions of said top stack-electrode layer, said dielectric thin film, said bottom electrode layer, and said conductive oxygen-diffusion barrier layer, thereby forming a capacitor stack comprising a top stack-electrode, a dielectric thin film, a bottom electrode, and a conductive oxygen-diffusion barrier, said conductive oxygen-diffusion barrier being in electrical contact with said top end of said conductive plug, said capacitor stack comprising a stack sidewall, and said top stack-electrode having a top surface.

Claim 45 (Original) A method as in claim 44, further comprising:

forming a third insulator layer on said substrate, thereby depositing a portion of said third insulator layer on said stack sidewall and on said second insulator layer;

removing a portion of said third insulator layer completely from at least a contact portion of said top surface of said top stack-electrode;

thereafter forming a top plate-line electrode layer on said contact portion of said top

stack-electrode and on said third insulator layer;

removing a portion of said top plate-line electrode layer from a switch area of said substrate;

removing a portion of said third insulator layer from said switch area of said substrate; and

removing a portion of said second insulator layer from said switch area of said substrate;

thereby exposing an exposed portion of said buried diffusion barrier layer on a bit-line side of said capacitor stack, and further thereby forming a protected sidewall, said protected sidewall comprising a plate-line edge, top stack-electrode edge, a dielectric thin film edge, a bottom electrode edge, a conductive oxygen-diffusion barrier edge, and a second insulator layer edge.

Claim 46 (Original) A method as in claim 45, further comprising forming a nonconductive hydrogen-diffusion barrier layer on said top plate-line electrode, on said protected sidewall, and on said exposed portion of said buried diffusion barrier layer.

Claim 47 (Original) A method as in claim 45, further comprising removing a portion of said nonconductive hydrogen barrier layer from a nonmemory area of said substrate.

Claim 48 (Original) A method as in claim 45, further comprising:

forming a fourth insulator layer on said substrate;

forming an electrical connection to said top plate-line electrode remotely from said capacitor stack; and

forming an electrical connection to said switch.

Claim 49 (Original) A method of fabricating an integrated circuit, comprising:

providing a substrate, said substrate comprising a switch and a capacitor stack, said capacitor stack comprising a top stack-electrode, a thin film of capacitor dielectric, a bottom electrode, and a conductive oxygen-diffusion barrier, said conductive oxygen-diffusion barrier located above said switch;

forming a top plate-line electrode on said top stack-electrode; and

forming a continuous electrically nonconductive hydrogen-diffusion barrier layer on said plate-line electrode, on a protected side of said capacitor stack, and on a switch area of said substrate.

Claim 50 (Original) A method of fabricating a ferroelectric integrated circuit, comprising:

providing a substrate including a switch and a first insulator layer covering said switch;

forming a conductive plug through said first insulator layer, said conductive plug having a bottom end and a top end, said bottom end in electrical contact with said switch;

planarizing said top end of said conductive plug;

forming a stack of capacitor layers over said conductive plug, said stack including a bottom electrode layer, a thin film capacitor ferroelectric layer, and a top stack-electrode layer;

removing portions of said top stack-electrode layer, said ferroelectric thin film, and said bottom electrode layer, thereby forming a plurality of separated capacitor stacks, each comprising a top stack-electrode, a ferroelectric thin film, and a bottom electrode;

forming a capacitor insulator layer over said capacitor stacks, filling in said removed portions and thereby insulating said capacitor stacks from one another and protecting their sides;

removing a portion of said capacitor insulator layer from at least a contact portion of said top surface of said top stack-electrodes; and

thereafter forming a top plate-line electrode layer on said contact portion of said top stack-electrode and on said capacitor insulator layer.

Claim 51 (Original) A method as in claim 50 wherein said forming a stack of capacitor layers further comprises forming a conductive oxygen-diffusion barrier layer prior to forming said bottom electrode layer, and said removing portions of said top stack-electrode layer includes removing portions of said conductive oxygen-diffusion barrier layer.

Claim 52 (Original) A method as in claim 51 wherein said removing portions

of said top stack-electrode layer comprises:

depositing a hardmask on said top stack-electrode;

patterning said hardmask;

etching said top stack-electrode layer, said ferroelectric thin film, and said bottom electrode layer;

removing said hard mask; and

etching said barrier layer.

Claim 53 (Original) A method as in claim 50 wherein said top-stack electrode layer is from 5 nm to 100 nm thick.

Claim 54 (Original) A method as in claim 53 wherein said top-stack electrode layer is 50 nm thick.

Claim 55 (Original) A method as in claim 50 wherein said removing portions of said top stack-electrode layer comprises:

depositing a hardmask on said top stack-electrode;

patterning said hardmask;

etching said top stack-electrode layer, said ferroelectric thin film, and said bottom electrode layer; and

removing said hard mask.

Claim 56 (Original) A method as in claim 50 wherein removing a portion of said capacitor insulator layer comprises planarizing said capacitor insulator layer to expose said top stack-electrodes.

Claim 57 (Original) A method as in claim 50, and further comprising crystallizing said ferroelectric layer prior to said removing portions of said top stack-electrode layer, said ferroelectric thin film, and said bottom electrode layer.

Claim 58 (Original) A method as in claim 50, and further comprising crystallizing said ferroelectric layer after said removing portions of said top stack-electrode layer, said ferroelectric thin film, and said bottom electrode layer.

Claim 59 (Original) A method as in claim 50 wherein said forming a stack of capacitor layers comprises using a low-thermal-budget technique to form a thin film of

ferroelectric layer superlattice material having a thickness less than 100 nm, and heating said substrate at an elevated temperature exceeding 500°C for a cumulative heating time of less than five minutes.

Claims 60 – 66 (Canceled)